**Chapter 1**

**Introduction**

* 1. **Motivation: -**

Microelectronic products continue to connect and change to control our world in the 21st century thanks to unprecedented technological advances and rapid adoption in economic and industrial society. In addition to the successful parade of smartphones contemporary achievements such as activity trackers delivery drones and electric vehicles as well as bio-implants for driverless cars and ongoing innovations related to the Internet of Things will not only address many logistical and medical and environmental problems of Today. but they have profoundly revolutionized modern life in many respects.

Driven by a market demand for low-cost, multi-purpose, and densely integrated circuits (ICs), the semiconductor industry can be seen to follow a trend towards system-on-chip (SOC) solutions with a growing amount of mixed-signal content, i.e., both digital and analog IC sections. Due to the growing need for more computing power digital circuits have long been of great interest but now analog circuits are also of great interest., primarily incited by the desire for functional diversification and system integration. Amongst others, the soaring importance of sensor functionality and the sophistication of advanced human-machine interfaces make Analog circuit parts are more important.

Increasing chip complexity and shortening product lifecycles require electronic design automation in both the digital and analog domains to complete the task of creating IC designs. But even digital IC design follows a highly automated algorithm synthesis flow from the start. Analog circuits are typically produced by experienced designers with a low level of automation especially since the schematic design phase where the circuit diagram is converted to the actual implementation circuit is a major bottleneck in the overall design flow Figure (1.1).

Figure 1.1: Simplified illustration of the integrated circuit design flow.


Topic of this Thesis

Figure 1. 1: Simplified illustration of the integrated circuit design flow.

The task of verifying the system specification as an electronic circuit is a very creative act. This is especially true for the analog layout design steps that this paper focuses on. Analog layout design relies heavily on the intuitive experience and creativity of the designers involved and is therefore considered an art by many experts in the field. This is also reflected in Alan Hastings title The Art of Analog Layout [[[1]](#footnote-1)]. It is considered standard work in the analog display community. Unfortunately, these human characteristics cannot be easily automated on a scale that meets industrial needs.

In the past, layout design was done manually using drafting tools such as pencils, rulers, and compasses. The layout engineer would use these tools to draw the circuit on a sheet of paper or a Mylar film [BOPET] (Biaxially-oriented polyethylene terephthalate).

This process was a time-consuming and labor-intensive process that required a high level of skill and expertise. The layout engineer would need to visualize the circuit in three dimensions and create a layout that met the performance, reliability, and manufacturability requirements. As computer-aided design (CAD) technology advanced, the process of layout design began to be done using software. The first EDA layout tools were simple software programs that allowed designers to draw the schematic and layout of their circuits manually. However, these tools were limited in their functionality and were not very efficient.

Today, EDA layout tools have advanced significantly, and they are the primary means of layout design in the electronics industry. These tools use a combination of algorithms, heuristics, and user input to optimize the placement and routing of components on a circuit board, while taking into account factors such as signal integrity, thermal management, and manufacturing constraints. EDA layout tools have many advantages over manual layout. They are much faster and more efficient, and they can handle the increasing complexity of modern electronics design. They also provide a high level of accuracy and consistency, which is critical for ensuring the performance and reliability of the circuit. Overall, the evolution of layout design from manual layout in the past to the EDA tools that are used today has been driven by advances in computer hardware and software, as well as the increasing complexity of integrated circuits.

**The Problem of Analog Layout Design**

This section describes some aspects of analog layout design that are important for understanding the work presented here and introduces technical terms that will be covered in the rest of this thesis.

As mentioned in Section 1.1, the problem of analog layout design is to take a given electronic circuit and turn it into a physical representation, which is itself also called a layout design. The purpose of that physical representation is to describe the detailed chip geometries on the photolithographically masks which need to be created for the various layers of the semiconductor manufacturing process.

These geometries include the layout of the circuit components and their electrical interconnections with interconnect holes between isolating layers, as well as the so-called bond pads for the chip’s connections to its periphery, converting an electronic circuit into a practical layout requires consideration of many design restrictions and design objectives that arise from understanding the circuits’ function. Thus, the readability of a schematic diagram is not only for circuit designers but also for layout designers.

* + 1. **Design Restrictions and Design Objectives: -**

From a mathematical point of view, layout design is an optimization problem and can be regarded as a search for an optimal solution inside a huge solution space. Thereat, design restrictions define a valid region in the solution space, while the design objectives specify an optimum inside that valid region, as depicted in [[[2]](#footnote-2)]. Design restrictions are commonly divided into three categories:

* **Technological restrictions:** are meant to ensure the manufacturability of the (IC). They are derived from the chosen semiconductor technology and formulated as geometrical design rules. Design Rule Check (DRC) can be very complex, but most of them belong to one of the following groups: minimum width, minimum distance, minimum overlap, or minimum enclosure.
* **Functional restrictions** (electrical restrictions) are supposed to guarantee the circuit’s proper electrical functioning. They can be separated into circuit-specific requirements (e.g., to prevent unwanted coupling effects) and process-specific requirements (such as the limitation of current density in electrical wires to avoid electromigration).
* **Design-methodical restrictions** are deliberately introduced to reduce the complexity of the layout design problem, thereby making the design task amenable to computer-aided automation approaches. An example is given by layer-dependent wire directions for the purpose of automated routing (e.g., metal1: horizontal, metal2: vertical).

**Process Design Kit (PDK) and Design rules [[[3]](#footnote-3)]**

A **PDK** is a collection of files, libraries, and design rules that provide the information and tools necessary for designing ICs using a specific fabrication process. The PDK includes a range of design rule checks (DRCs) and layout versus schematic (LVS) checks to ensure that the layout of the IC meets the requirements of the fabrication process. The PDK also includes models for device simulation and characterization, allowing designers to simulate the behavior of the IC under different operating conditions.

**In our work we** use Saed\_pdk\_32\_28 is a Process Design Kit (PDK) developed by the Semiconductor Advanced Electronics Design **(SAED**) group at Ain Shams University in Egypt. it appears that the design rules for Saed\_pdk\_32\_28 are based on micron (µm) measurements, rather than lambda-based rules. Lambda-based rules are typically used in deep submicron processes, where the feature sizes are smaller than the wavelength of light used in photolithography. The 0.35 µm technology node is not considered a deep submicron process,

* 1. **Levels of Design Hierarchy**

Analog IC layouts are usually built in a hierarchical fashion, which is achieved by putting design components inside other design components. Basic design units such as transistors are usually provided as primitive devices i.e. basic cells with no sub-hierarchies. At a higher level a group of design elements that together form a functional unit can be contained in a single (but in a hierarchical case) cell. Functional units become modular library components that can be instantiated in layouts like base units. To avoid semantic confusion when talking about units it is best to classify them according to these characteristics based on their position in the design hierarchy , For that purpose, this thesis proposes and adheres to the following terminology

|  |  |  |  |
| --- | --- | --- | --- |
|  | Hierarchy Level | Examples | Degree of  (Re-)Utilization |
| Blocks | Block Level | Variable Gain Amplifiers (VGA) | Low |
| Advanced Modules | Module Level | Operational Transconductance Amplifiers (OTA), Differential Amplifiers, | Medium |
| Simple Module | Module Level | Differential Pairs, Current Mirrors, | High |
| Primitive Device | Devices Level | Transistors, Resistors, Capacitors, Guard rings | Very high |

table 1 : Classification of hierarchical cells in analog/mixed-signal design

* 1. **Main Design Tasks:  
      Device Generation, Floorplanning, Placement, Routing**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Floorplanning | Placement | Routing |
| Considered Components | Circuit Blocks (treated as black boxes) | Primitive Devices and Modules | Wire Segments + Vias (to cross metal layers) |
| Quantities to be set by the Design Task | * Block Locations * Aspect Ratios * Pin Positions | * Locations * Orientations * Layout Variants | Wire Paths, Segment Layers and Widths + Via Positions and Sizes |
| Typical Restrictions | * Rect. Chip Outline * Block Distances * Chip Regions | * Block Outline * Space for Routing * Parasitics | * No Wires Above Devices * Available Metal Layers * Parasitics and Currents |
| Primary Objectives | * Minimize Area and Wirelength * Optimize Power Supply and Current Flow | Device Matching | Minimize Number of Vias and Number of Metal Layers |

Table 1 The main tasks in analog layout design

* + 1. **Device Generation**

in layout refers to n is the task of creating the layouts for the individual components of the given input circuit. Here for, every component needs to be individually layouted according to its respective sizing (e.g., the channel width and channel length of a MOS transistor). In the past, this task has been an integral duty on the shoulders of an IC design team.

Today it is common practice that the primitive devices of a semiconductor technology are readily delivered by the vendor as part of a so-called process design kit (PDK), which is involves creating the metal interconnects, transistors, and other components that make up the circuit, and optimizing their placement, spacing, and routing to meet the requirements of the technology node. It is an iterative process that involves simulation, testing, and optimization.

Designers use simulation tools to model the performance of the circuit and identify potential layout issues, such as parasitics or timing violations. They then make adjustments to the layout, such as changing the placement of components or adjusting the width of metal interconnects, and test the circuit again to verify that the changes have improved its performance.

Device generation in layout is a critical step in the design of integrated circuits, as it determines the physical structure of the circuit and its performance characteristics.

Even primitive devices have an immense layout variability, and one major source of this variability is device folding. For example, a MOS transistor can be folded by changing its so-called number of fingers. As shown in Figure 2.1, the transistor variants thus have different aspect ratios while preserving the total channel width and channel length. Device generation is already important during floorplanning for estimating the total size of a layout block.

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تم إنشاء الوصف تلقائياً

figure : Different layout variants of a MOS transistor with the same total channel width and length.

In VLSI fingers and multipliers are two terms used to describe the layout transistors. finger means how many gates a transistor has while multiplier is how many times a transistor is replicated. Splitting transistors can either be done by using multiple transistors with a single gate” multiplier” or with transistors that have multiple gate “fingers”. When laying out a MOSFET with a particular width and length, in an EDA tool, one has two options with regards to the **shape of the gate**:

1. **Single stripe** (classical case) (one finger);
2. **Several stripes** (several fingers).

**advantages and disadvantages** of a transistor layout with **multiple fingers** (MF) vs **single finger**?

1) MF provide more **flexibility** in layout planning for transistor with high W/L or L/W. In other words, allows making a layout more square-like.

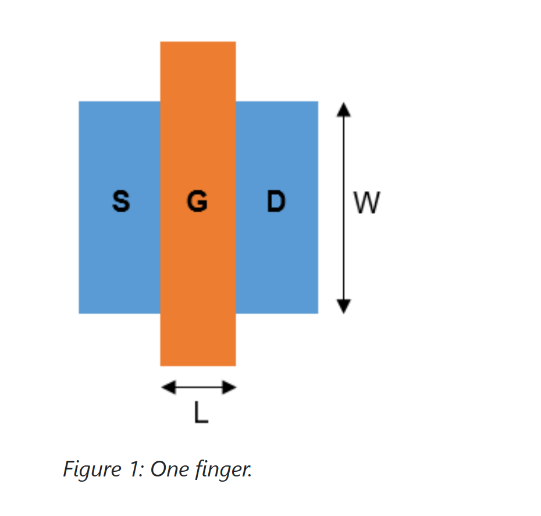
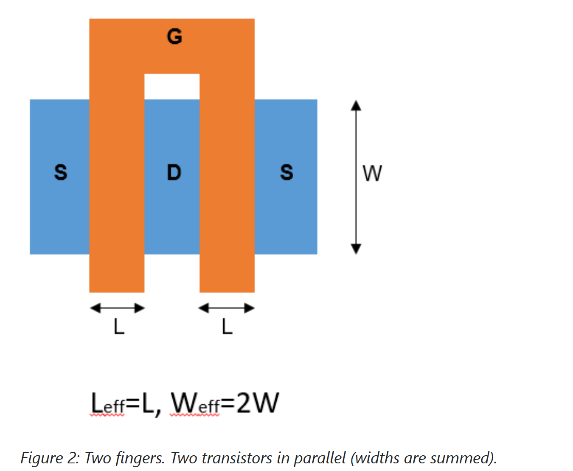
2) MF allow better **matching** of transistors, when needed. For example, if using common-centroid techniques.

3) MF layout **reduces gate resistance**.

4) MF **reduce current density** in the gate if there are technology limitations on this

**Transistors with multiple fingers have the disadvantages also:**

1. the current direction is different for two neighboring fingers. E.g., if for the first finger the source is to the left then the source for the next finger will be to the right.
2. The properties of transistor can change depending on the current direction. Therefore, extra care has to be taken when trying to achieve good matching.
3. Using multiple fingers to obtained scaled current sources for example in a current mirror is also considered inferior to having multiple single gate transistors because of slightly different properties.



* + 1. **Floorplanning**

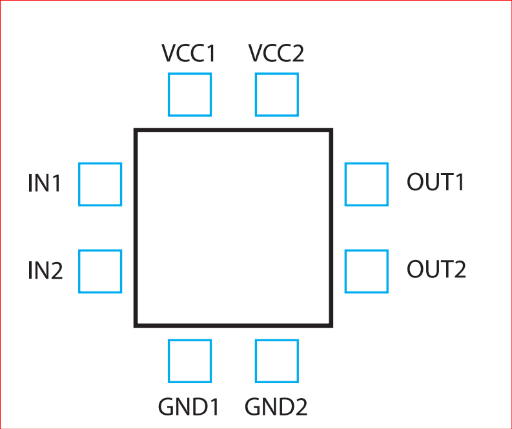
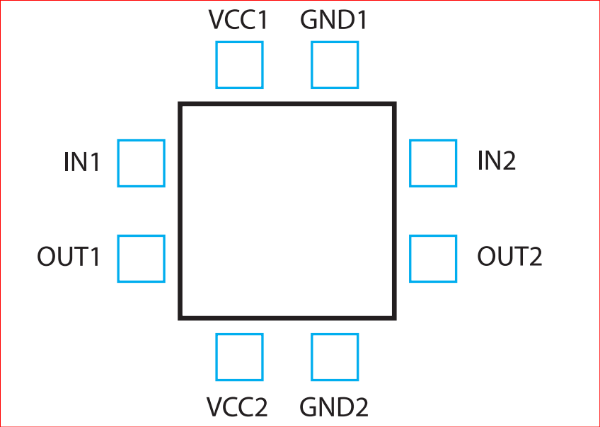
is the task of specifying locations, aspect ratios, and pin positions for the layout blocks of a chip. Therein, each block is treated as a black box whose area is roughly estimated by the floorplan designer from generating the block’s devices. For economical and electrical reasons, the primary objectives in floorplanning are to minimize the total layout area and the total wirelength, as well as to optimize the power supply and the current flow. A hard restriction concerning the layout area can be that the blocks must fit into a fixed outline, depending on the semiconductor package chosen for the physical sealing of the chip during the final stage of the fabrication. In general, the top-level chip boundary is demanded to be a rectangle whose aspect ratio should not depart too far from a square. In the context of wirelength minimization, some blocks are required to be positioned close to the chip boundary because they will later be connected with the periphery. On the other hand, it may also be necessary to keep a certain minimal distance between dedicated blocks such that sensitive signals are not disturbed by unwanted thermal and electrical influences. A large block can contain subordinate blocks that also need to be floor planned.

**Pin-Driven Planning:**

The pin-out is the first step of your floorplan in which you may participate as a mask designer. Some refer to it as the pad-out. This is the process in which the input and output pins that will surround the chip in its packaging are defined.

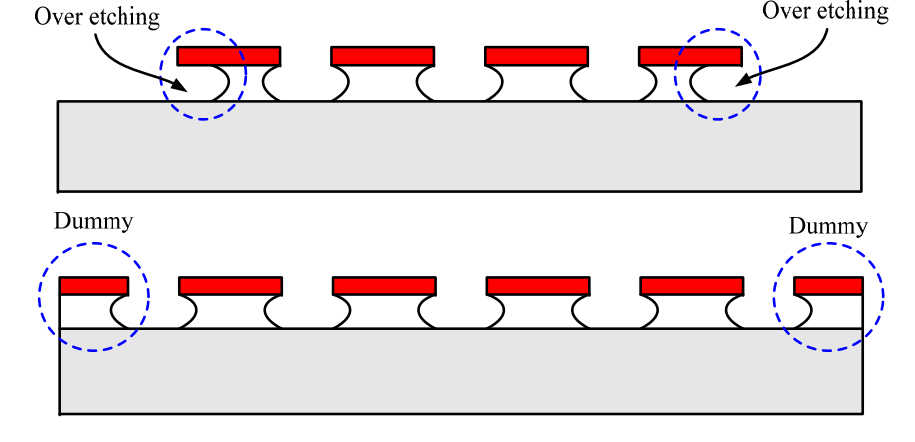
The pin-out directly affects your work. The quality of your pin-out directly affects how good your chip floorplan will be and how easy the chip will be to layout.

**You could use the same package and the same signals, but use the various signals to be in very different places. Very different pins placement will produce a very different layout as same as in the next figures.**



**To Obtain A good floorplanning [5] :**

* Start thinking about the layout when doing the schematics. Think about how this schematic translates to the layout.
* Industrial quality layout.
* Compact rectangular layout.
* Input and output on the two sides.
* VDD and VSS on the top and bottom.
* N-well all around
* User-defined connectivity requirements for every layer, in addition to net-based routing constraints, handle the results of analogue signal crosstalk, minimum capacitance, and resistance.
* Understands the various divisions or blocks of a design.
* Understands the important features of each block: size, aspect ratio, and pins.
* Dynamically displays the connectivity between blocks and connections to the pads.
* Allocates space for routing based on the number of routing layers.
* Places each block and optimizes the pin locations for each block based on the overall connectivity requirements and the feasibility of routing the signals between blocks.
* Places top-level ports based on constraints. floorplan made the electron’s life travels from one side to the other easier.
* Use dummy elements to improve symmetry and avoid Gate Etching Effect.



* Matched transistors are used extensively in both analog and digital CMOS circuits.
* Keep sufficient spacing between power blocks and sensitive blocks.
* Use Guard rings for isolation and guard Ring is a useful tool to protect our circuits from parasitic effects and so that chances of latch-up are reduced.

**Neat fly lines indicate good floor planning [5]:**

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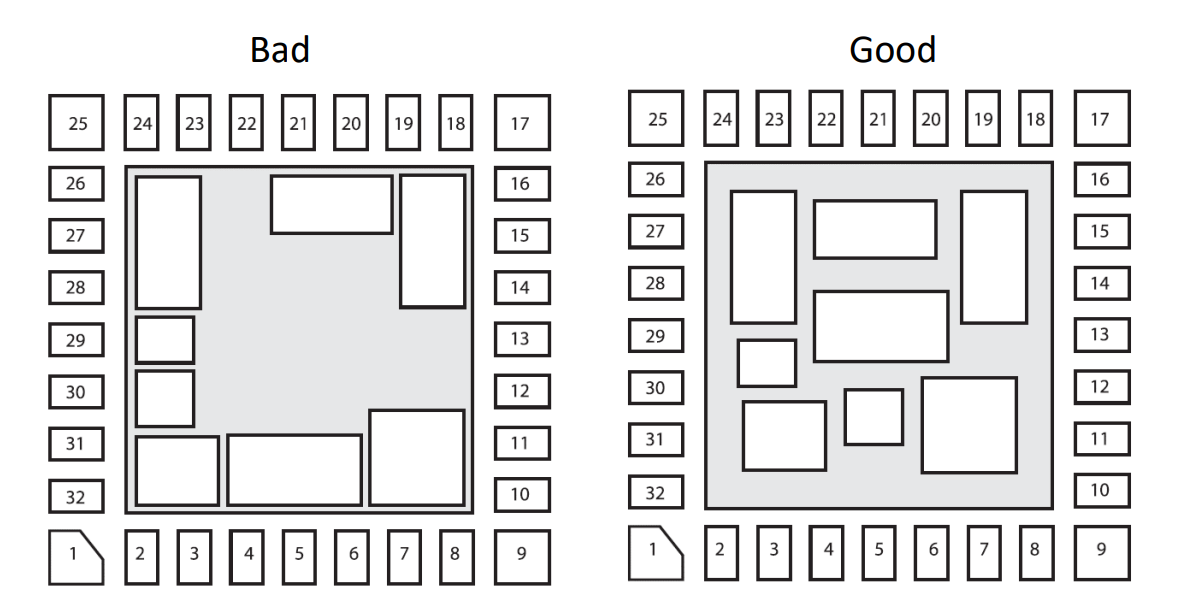
تم إنشاء الوصف تلقائياً**صورة تحتوي على نص, رسم بياني, خط, لقطة شاشة

تم إنشاء الوصف تلقائياً

Bad

Good

* + Minimize The area as possible is Perfect but be care to leave a good space for routing and decoupling caps.



* + Inputs and outputs should be placed near the correct cell blocks.
    1. **Placement:** it is not only means to move the layout components into appropriate locations, but may also require to rotate them and to vary their layout without affecting their electrical function (for example by changing the number of fingers discussed above), such that all components fit into the block outline defined during the floorplanning phase. As in floorplanning, it is desired to obtain a device placement wherein the total area and wirelength are minimized, but usually these objectives first and foremost stem from the need to obtain a good device matching. The same is true for higher-level modules whose placement aims at achieving an overall symmetry of the layout block where the modules are placed in. Opposing the need to place the components close to each other, a common demand is that a sufficient amount of space must be reserved between the components to accommodate their routing.
    2. **Routing:** refers to the process of creating the physical connections between the various components of an electronic circuit. This involves designing the metal interconnects that link the transistors, resistors, capacitors, and other components of the circuit, and optimizing their placement and routing to meet the specific requirements of the design. Routing in layout is a critical step in the design of electronic circuits, as it determines the physical structure of the circuit and its performance characteristics. The routing process involves creating the metal tracks that connect the different components of the circuit, and optimizing their placement and routing to minimize parasitic effects such as resistance, capacitance, and inductance.

The demand to allow for routing space between layout components is rooted in the fact that sensitive circuitry often forbids electrical wires to be drawn above these components. this has to be taken into account during the routing task. Another restriction is to confine which metal layers are available for the routing. On the lower design levels, a common agreement is that only the first two (M2 , M3 ) of the available metal layers may be used in order to retain the remaining metal layers for the later top-level routing. Leading a wire across different metal layers requires to connect the respective wire segments with a VIA (vertical interconnect access). The size of a via and the width of a wire segment must be set with respect to the expected current load.

**Primary objectives in routing are:**

* + to minimize the number of vias (i.e., to avoid crossing between metal layers if possible),
  + to minimize the number of metal layers (and thus the number of necessary photolithographically masks),

**Some important Rules which should follow in Routing:**

* Choose routing layers based on process parameters and circuit requirements. For each process a standardized list of routing layers should be determined based on layer resistance and capacitance. Layers such as N-well, active, and high-resistance poly gate are not used for routing.
* Priorities between routing layers can also be standardized using the same criteria [5].
* Use of more numbers of columns and rows vias.
* The use of metals with an odd number for vertical wires and an even number for horizontal wires to avoid interference between metals and each other.
* Minimize total run time for carrying out routing process [5].
* Minimize total wire length.
* Avoid too much parallel routing of metals (to decrease parasitic capacitance [5].
* Increase the width of the wire to overcome Electro migration [6].

**صورة تحتوي على لقطة شاشة, مستطيل, ميدان/ مربع, نص

تم إنشاء الوصف تلقائياًManhattan routing rule**: also known as the Manhattan style or Manhattan distance, is a common technique used in analog layout design to route interconnects between components. It is named after the street layout of Manhattan, which is characterized by a grid of perpendicular streets. The Manhattan routing rule involves routing interconnects in a series of right-angled, orthogonal segments, either horizontally or vertically. This ensures that the interconnects are parallel to the edges of the layout grid and minimizes parasitics such as capacitance and inductance. Using it also to reduce the common area between metal layers. For example, if Metal 1 is routed in horizontal direction. Is required to route M2 in vertical direction as shown in Figure (1.3)

Figure 1. 3 Manhattan routing rule

While design restrictions are strict confinements which must definitely be satisfied, design objectives represent gradual optimization goals that are pursued as good as possible. They can be roughly classified into economic optimization goals and functional optimization goals. Economic optimization goals include the reduction of product costs (e.g., by minimizing the total chip area and the number of required metallization layers) as well as reducing the development costs (e.g., by minimizing the design effort via design automation). Examples for functional optimization goals are the minimization of the total wirelength as well as optimizing the chip’s heat dissipation to prevent critical hot spots. One of the key advantages of the Manhattan routing rule is that it is easily automated using computer-aided design (CAD) tools. This allows designers to quickly and efficiently route interconnects in complex circuits, saving time and reducing errors. However, the Manhattan routing rule also has some limitations. For example, it may not be the most efficient routing strategy for certain types of circuits, such as those with high-frequency signals or those with non-orthogonal components .[[[4]](#footnote-4)]

As the name implies, functional restrictions and functional optimization goals pertain to the functionality of an integrated circuit. Herein, three basic issues can be embraced by the term functionality:

* Does the circuit work accurately enough to perform the desired function?
* How well is the circuit set up against long-term failure owing to effects of degradation?
* What measures are taken to prevent an instantaneous malfunctioning due to fabrication problems?   
  **The answer of those issues will be postponed to chapter 3** 
  1. **Physical Verification**

After the physical design is complete the layout must be fully verified to ensure correct electrical and logical functionality (correctness of a physical layout design with respect to the design rules and specifications), It is an essential step in the semiconductor manufacturing process, as it ensures that the final product will function correctly and meet the desired performance criteria. The physical verification process involves checking various parameters such as the width and spacing of metal and poly lines, the alignment of cells, and the presence of shorts and opens. The verification process is performed using various tools and techniques such as:

* **Design rule checking (DRC):** verifies that the layout meets all technology-imposed constraints. These rules include the following categories: -
* Typical geometrical design rules that require minimum or maximum values for widths, spacings, extensions, intrusions, and enclosures for layout polygons. These rules make sure that the layout structures can be correctly generated on the silicon due to process accuracy
* **Layout versus schematic (LVS)**: is checking that the design is connected correctly. The schematic is the reference circuit and the layout is checked against it. In principle, the following is verified:
* Electrical connectivity of all signals, including input, output, and power signals to their corresponding devices
* Device sizes: transistor width and length, resistor sizes, capacitor sizes.
* Identification of extra components and signals that have not been included in the schematic; floating nodes would be an example of this. The last item overlaps into the items checked in the electrical rules check, which is described previous
* **Parasitic extraction (PEX):** is extracting the parasitic effects of interconnects and devices in a chip. Parasitic effects are unwanted electrical characteristics that arise due to the physical properties of the components used in the chip design. These effects can cause delays, noise, and other performance issues that can impact the functionality of the chip.

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